AMENDMENTS TO THE CLAIMS

1. (Original) A digital signal processor comprising:

a core processor;

a level one memory for operation with the core processor;

a store buffer configured to hold write information, generated by the core processor, for the level one memory and for a level two memory, the store buffer having a store buffer capacity;

a write buffer configured to hold write information, received from the store buffer, for the level two memory, the write buffer having a normal capacity and an excess capacity; and

a memory controller configured to enable the excess capacity of the write buffer when a high priority task is being serviced and to inhibit write access to the excess capacity of the write buffer when a high priority task is not being serviced.

2. (Original) A digital signal processor as defined in claim 1, wherein the high priority task is an interrupt handler.

3. (Original) A digital signal processor as defined in claim 1, wherein the excess capacity of the write buffer is equal to or greater than the effective store buffer capacity.

4. (Original) A digital signal processor as defined in claim 1, wherein the memory controller is configured to transfer the contents of the store buffer to the write buffer when the high priority task is invoked.

5. (Original) A digital signal processor as defined in claim 4, wherein the memory controller is configured to stall the core processor when the high priority task is completed and to write the contents of the write buffer to memory until the write information held in the write buffer no longer uses the excess capacity.

6. (Original) A digital signal processor as defined in claim 5, wherein the memory controller is configured to increase the priority of write operations to the level two memory when the core processor is stalled following completion of a high priority task.

7. (Original) A digital signal processor as defined in claim 1, further comprising a second write buffer configured to hold write information for a level three memory and to receive the write information from the first-mentioned write buffer.

8. (Original) A digital signal processor comprising:

a core processor;

a relatively fast memory for operation with the core processor;

a store buffer configured to hold write information, generated by the core processor, for the relatively fast memory and for a relatively slow memory, the store buffer having a store buffer capacity;

a write buffer configured to hold write information, received from the store buffer, for the relatively slow memory, the write buffer having a normal capacity and an excess capacity; and

a memory controller configured to enable the excess capacity of the write buffer and to transfer contents of the store buffer to the write buffer when a high priority task is invoked and to inhibit write access to the excess capacity of the write buffer when a high priority task is not being serviced.

9. (Original) A digital signal processor as defined in claim 8, wherein the high priority task is an interrupt handler.

10. (Original) A digital signal processor as defined in claim 8, wherein the excess capacity of the write buffer is equal to or greater than the effective store buffer capacity.

11. (Original) A digital signal processor as defined in claim 8, wherein the memory controller is configured to stall the core processor when the high priority task is completed and to write the

contents of the write buffer to memory until the write information held in the write buffer no longer uses the excess capacity.

12. (Original) A digital signal processor as defined in claim 11, wherein the memory controller is configured to increase the priority of write operations to the relatively slow memory when the core processor is stalled following completion of a high priority task.

13. (Original) A method for operating a digital signal processor comprising:

providing a digital signal processor including a core processor, a level one memory for operation with the core processor, and a store buffer configured to hold write information for the level one memory and for a level two memory;

providing a write buffer, configured to hold write information, received from the store buffer, for the level two memory, having a normal capacity and an excess capacity;

enabling the excess capacity of the write buffer and transferring the contents of the store buffer to the write buffer when a high priority task is invoked; and

inhibiting write access to the excess capacity of the write buffer when a high priority task is not being serviced.

14.-29. (Canceled)

30. (Currently amended) A digital signal processor comprising:

a core processor;

a level one memory for operation with the core processor;

a store buffer configured to hold write information, generated by the core processor;

a first write buffer configured to hold write information, received from the store buffer, for a level two memory;

a second write buffer configured to hold write information, received from the store buffer, for a level three memory; and

a memory controller configured to steer write information to the first write buffer or the second write buffer based on an address of a write operation, wherein at least one of the write buffers has a normal capacity and an excess capacity and wherein the memory controller is configured to enable the excess capacity when a high priority task is being serviced and to inhibit write access to the excess capacity when a high priority task is not being serviced.

31. (Canceled)

32. (Currently amended) A digital signal processor as defined in claim [[31]] 30, wherein the high priority task comprises an interrupt handler.

33. (Currently amended) A digital signal processor as defined in claim [[31]] 30, wherein the excess capacity is equal to or greater than an effective capacity of the store buffer.

34.-36. (Canceled)